**Curriculum Vitae**

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| **1.Personal Information** |  |
| **Name** | Basim Yousef Alshar' |
| **Nationality** | Jordanian |
| **Contact Information** | Computer Engineering Dept.Faculty of Engineering Mu’tah UniversityKarak, JORDAN 61710Email: b@mutah.edu.jo |

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| **2.Academic Qualifications** |
|  | **University** | **Year** | **Country** | **Major** |
| **B.A** | **Jordn university of science and****technology** | **2002** | **Jordan** | **Computer Engineering** |
| **M.A** | **Jordn university of science and****technology** | **2007** | **Jordan** | **Computer Engineering** |
| **Ph.D** |  |  |  |  |

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| **3.Research and Teaching Interests** |
| **Computer architecture** |
| **VLSI transistor level circuit design** |
| **Digital Logic Design** |
| **Network and Computer Security** |
| **Electronics and Digital Electronic** **Circuits** |

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| **4.Articles** |
| **Title** | **Publication Date** | **Journal/ Conference** | **Volume** | **Pages** |
| Delay and PerformanceEstimation for a 4-bit EvenParity Bit Generator Using theLogical Effort Model. | 2015 | International Reviewon Computers andSoftware ( IRECOS) | 10(8) | 814-819 |